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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,288	09/19/2001	Joo-Hyong Lee	LGS/S-0030A	9373

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,288	LEE, JOO-HYONG	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 11-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 11-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/290,891* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

➢ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 20, 2003 has been entered.

Claim Objections

➢ Claim 21 is objected to because of the following informalities:

- Last two lines of the claim: please identify the heavily doped region as to be the one having the second conductivity type.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

➢ Claims 1-2, 4-5 and 11-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong (US Patent No. 6,232,165 B1).

Regarding claims 1 and 26, Wong teaches a semiconductor device comprising: a semiconductor substrate (4) having a first conductivity type (P-) (see Fig. 1); a first well (6) having a second conductivity type (N-) formed in a first region in a major surface of the semiconductor substrate (see Fig. 1); a first MOS transistor (18, 20, 24) having the first conductivity type (P) (see Fig. 1) and a first contact region (consider the heavily doped portion over the region 22) having the second conductivity type (N+) formed in the first well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (22) having the second conductivity type (N+) formed between the first contact region (consider the heavily doped portion over the region 22) in the first well (6) and a surface (consider the junction line at the bottom surface of the first well and adjacent to the substrate) of the first well (6) opposite from the first contact region within the semiconductor substrate (4) (see Figs. 1 and 2G-2H).

Regarding claim 2, Wong teaches a second well (8) having a second conductivity type (P-) formed in a second region in a major surface of the semiconductor substrate (see Fig. 1); a second MOS transistor (10, 12, 24) having the second conductivity type (N) and a second contact region (consider the heavily doped portion over the region 16) having the second conductivity type (P+) formed in the second well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (16) having the first conductivity type (P) formed between the second contact region (consider the heavily doped portion over the region 16) in the second well (8) and a surface (consider the junction line at the

bottom surface of the second well and adjacent to the substrate) of the second well (8) opposite from the second contact region within the semiconductor substrate (4) (see Fig. 1 and 2G-2H).

Regarding claims 4 and 18, Wong teaches that the concentration of the heavily doped region of buried layer (16) having the first conductivity type (**P+**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{12} per cm^2) is higher than that of the second well (**P**) and lower than that of the second contact region (**P++**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{14} per cm^2) (see Figs. 1 and 2G-2H, and col. 4, lines 37-38 and 62-65 and col.5, lines 34-36).

Regarding claims 5 and 19, Wong teaches that the concentration of the heavily doped region of buried layer (22) having the second conductivity type (**N+**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{12} per cm^2) is higher than that of the first well (**N**) and lower than that of the first contact region (**N++**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{14} per cm^2) (see Figs. 1 and 2G-2H, and col. 4, lines 33-34 and 52-55 and col.5, lines 49-51).

Regarding claims 12 and 23, Wong teaches that the heavily doped region (22) of the second conductivity type (N+) does not extend under the first MOS transistor (18, 20, 24) in the first well (6) (see Figs. 1 and 2G-2H).

Regarding claim 13, Wong further teaches a second well (8) having a first conductivity type (P) formed in a second region of the semiconductor substrate (4),

wherein the heavily doped region of buried layer (22) having a second conductivity type (N+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claim 14, Wong further teaches a second well (8) having a first conductivity type (P) formed in a second region of the semiconductor substrate (4), and a heavily doped region of buried layer (16) having a first conductivity type (P+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claims 15-16 and 28, Wong teaches a semiconductor substrate (4) having a first conductivity type (P), a first well (6) having a second conductivity type (N) formed in a first region of the semiconductor substrate (4), a second well (8) having a first conductivity type (P) formed in a second region of the semiconductor substrate (4) (see Fig. 1), and a heavily doped region of buried layer (22) having a second conductivity type (N+) not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface), wherein the buried layer (22) is within the semiconductor substrate (4) separated from any surfaces of the semiconductor substrate. See Fig. 2G.

Regarding claim 17, Wong further teaches a heavily doped region of buried layer (16) having a first conductivity type (P+) not formed at an interface between the first and

second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claims 24 and 30, Wong teaches a semiconductor device comprising: a semiconductor substrate (4) having a first conductivity type (P-) (see Fig. 1); a first well (6) having a second conductivity type (N-) formed in a first region in a major surface of the semiconductor substrate (see Fig. 1); a first MOS transistor (18, 20, 24) having the first conductivity type (P) (see Fig. 1) and a first contact region (consider the heavily doped portion over the region 22) having the second conductivity type (N+) formed in the first well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (22) having the second conductivity type (N+) formed between the first contact region (consider the heavily doped portion over the region 22) in the first well (6) and an outer surface (consider the junction line at the bottom surface of the first well and adjacent to the substrate) of the first well (6) within the semiconductor substrate (4) (see Figs. 1 and 2G-2H). Furthermore, Wong teaches a second well (8) having a second conductivity type (P-) formed in a second region in a major surface of the semiconductor substrate (see Fig. 1); a second MOS transistor (10, 12, 24) having the second conductivity type (N) and a second contact region (consider the heavily doped portion over the region 16) having the second conductivity type (P+) formed in the second well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (16) having the first conductivity type (P) formed between the second contact region (consider the heavily doped portion over the region 16) in the second well (8) and an outer surface (consider the junction line at the bottom surface of the second well and adjacent to the substrate) of the second well

(8) within the semiconductor substrate (4) (see Fig. 1 and 2G-2H). In addition, Wong teaches that the heavily doped region of buried layer (22) having a second conductivity type (N+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface); and also, that the heavily doped region of buried layer (16) having a first conductivity type (P+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claims 27, 29 and 31, Wong teaches that the heavily doped region of buried layer (16, 22) prevents latch-up (see col. 3, lines 14-23).

➢ Claims 1-5, 11, 13-22 and 24-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Han et al. (US Patent No. 5,831,313).

Regarding claims 1 and 26, Han et al. teach a semiconductor device comprising: a semiconductor substrate (210) having a first conductivity type (N) (see Fig. 6); a first well (212) having a second conductivity type (P) formed in a first region in a major surface of the semiconductor substrate (see Fig. 6); a first MOS transistor (G201) having the first conductivity type (N) (see Fig. 6) and a first contact region (228) having the second conductivity type (P+) formed in the first well (see Fig. 6); and a heavily doped region of buried layer (HDR1) having the second conductivity type (P) formed between the first contact region (228) in the first well (212) and a surface (262) of the

first well (212) opposite from the first contact region within the semiconductor substrate (210) (see Fig. 6).

Regarding claim 2, Han et al. teach a second well (214) having a second conductivity type (N) formed in a second region in a major surface of the semiconductor substrate (see Fig. 6); a second MOS transistor (G202) having the second conductivity type (P) and a second contact region (230) having the second conductivity type (N+) formed in the second well (see Fig. 6); and a heavily doped region of buried layer (HDR2) having the first conductivity type (N) formed between the second contact region (230) in the second well (214) and a surface (264) of the second well (214) opposite from the second contact region within the semiconductor substrate (210) (see Fig. 6).

Regarding claim 3, Han et al. teach a depth of about 1.5 to 2.0 μm (see Fig. 6).

Regarding claims 4 and 18, Han et al. teach that the concentration of the heavily doped region of buried layer (HDR2) having the first conductivity type (N) is higher than that of the second well (214) (see col. 6, lines 61-63) and lower than that of the second contact region (230) (see Fig. 6).

Regarding claims 5 and 19, Han et al. teach that the concentration of the heavily doped region of buried layer (HDR2) having the second conductivity type (P) is higher than that of the first well (212) and lower than that of the first contact region (228) (see Fig. 6).

Regarding claims 11, 20, 21-22, and 25, Han et al. teach that the buried layers (HDR1 and HDR2) are separated from the contact regions (228 and 230). See Fig. 6.

Regarding claim 13, Han et al. further teach a second well (214) having a first conductivity type (N) formed in a second region of the semiconductor substrate (210), wherein the heavily doped region of buried layer (HDR1) having a second conductivity type (P) is not formed at an interface between the first and second wells (227). See Fig. 6.

Regarding claim 14, Han et al. further teach a second well (214) having a first conductivity type (N) formed in a second region of the semiconductor substrate (210), and a heavily doped region of buried layer (HDR2) having a first conductivity type (N) is not formed at an interface between the first and second wells (227). See Fig. 6.

Regarding claims 15-16 and 28, Han et al. teach a semiconductor substrate (210) having a first conductivity type (N), a first well (212) having a second conductivity type (P) formed in a first region of the semiconductor substrate (212), a second well (214) having a first conductivity type (N) formed in a second region of the semiconductor substrate (210) (see Fig. 6), and a heavily doped region of buried layer (HDR1) having a second conductivity type (P) not formed at an interface between the first and second wells (227), wherein the buried layer (HDR1) having the second conductivity type (P) is within the semiconductor substrate (210) separated from any surfaces of the semiconductor substrate. See Fig. 6.

Regarding claim 17, Han et al. further teach a heavily doped region of buried layer (HDR2) having a first conductivity type (N) not formed at an interface between the first and second wells (227). See Fig. 6.

Regarding claims 24 and 30, Han et al. teach a semiconductor device comprising: a semiconductor substrate (210) having a first conductivity type (N) (see Fig. 6); a first well (212) having a second conductivity type (P) formed in a first region in a major surface of the semiconductor substrate (see Fig. 6); a first MOS transistor (G201)) having the first conductivity type (N) (see Fig. 6) and a first contact region (228) having the second conductivity type (P) formed in the first well (see Fig. 6); and a heavily doped region of buried layer (HDR1) having the second conductivity type (P) formed between the first contact region (228) in the first well (212) and an outer surface 262) of the first well (212) within the semiconductor substrate (210) (see Fig. 6). Furthermore, Han et al. teach a second well (214) having a second conductivity type (N) formed in a second region in a major surface of the semiconductor substrate (see Fig. 6); a second MOS transistor (G202) having the second conductivity type (P) and a second contact region (230) having the second conductivity type (N) formed in the second well (see Fig. 6); and a heavily doped region of buried layer (HDR2) having the first conductivity type (N) formed between the second contact region (230) in the second well (214) and an outer surface (264) of the second well (214) within the semiconductor substrate (210) (see Fig. 6). In addition, Han et al. teach that the heavily doped region of buried layer (HDR1) having a second conductivity type (P) is not formed at an interface between the first and second wells (227); and also, that the heavily doped region of buried layer (HDR2) having a first conductivity type (N) is not formed at an interface between the first and second wells (227). See Fig. 6.

Regarding claims 27, 29 and 31, Han et al. teach that the heavily doped region of buried layer (HDR 1 and HDR2) prevents latch-up (see Fig. 6 and Abstract).

Response to Arguments

➢ Applicant's arguments with respect to claims 1-5 and 11-31 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

EDDIE LEE
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JRD
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